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08/28/03

U.S. PATENT AND TRADEMARK OFFICE
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

In re Application of: **LO IACONO**
Serial No.: **Not yet assigned**
Filed: **Herewith**
For: **METHOD AND RELATIVE CIRCUIT FOR INCREMENTING,
DECREMENTING OR TWO'S COMPLEMENTING A BIT
STRING**

Sir:

Transmitted herewith is an INFORMATION DISCLOSURE STATEMENT in the above-identified application.

1. This IDS is submitted under 37 C.F.R. § 1.97. No fee is required.
2. This IDS is submitted under 37 C.F.R. § 1.97(c). Enclosed is a check in the amount of \$180.00.
3. This IDS is submitted under 37 C.F.R. § 1.97(c) and (e). No fee is required.
4. This IDS is submitted under 37 C.F.R. § 1.97(d) and (e). Enclosed is a check in the amount of \$130.00 to cover the petition fee.
5. The Commissioner is hereby authorized to charge or credit any discrepancies in fee amounts to Deposit Account No. 01-0484.
6. Please associate this application with Customer No. 27975.



PATENT TRADEMARK OFFICE

Date: August 28, 2003


MICHAEL W. TAYLOR
Reg. No. 43,182

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: LO IACONO)
Serial No. Not yet assigned)
Filing Date: Herewith)
For: METHOD AND RELATIVE CIRCUIT)
FOR INCREMENTING, DECREMENTING))
OR TWO'S COMPLEMENTING A BIT)
STRING)
I HEREBY CERTIFY THIS PAPER OR FEE IS BEING
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PATENT APPLICATION, PO BOX 1450,
ALEXANDRIA, VA 22313-1450.
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DATE OF DEPOSIT: August 28, 2003
NAME: Kristin Thanski
SIGNATURE: Kristin Thanski

CITATION UNDER 37 CFR §1.97

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

Sir:

Attached is Form PTO-1449 listing several references for consideration in the examination of the above-identified application. A copy of each reference is also enclosed. It is requested that these references be considered by the Examiner and officially made of record in accordance with the provisions of 37 CFR §1.97 and Section 609 of the MPEP.

Respectfully submitted,


MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407/841-2330
Attorney for Applicant

INFORMATION DISCLOSURE STATEMENT			Atty Docket: Serial No.: Applicant: Filing Date: Group:	02CT17653403 Not Yet Assigned LO IACONO Herewith				
U.S. PATENT DOCUMENTS								
Examiner Initials		Document Number	Date	Name	Class	Sub Class	Filing Date	
	AA	4,534,010	8/6/85	Kobayashi et al.	364	748		
	AB	5,146,479	9/8/92	Okada et al.	377	41		
	AC	5,333,120	7/26/94	Gilber't	364	786		
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Sub Class	Translation	
	AK							
	AL							
	AM							
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)								
	AN	Hashemian et al., A New Parallel Technique for Design of Decrement/Increment and Two's Complement Circuits, Proceedings of the Midwest Symposium on Circuits and Systems, Monterey, May 14-17, 1991, New York, US, Vol. 2 Symp. 34, May 14, 1991, Pages 887-890, XP000333546						
	AO	Sone et al., A 10-b 100-Msample/s Pipelined Subranging BiCMOS ADC, IEEE Journal of Solid-State Circuits, IEEE Inc. New York, US, Vol. 28, No. 12, December 1, 1993, Pages 1180-1186, XP000435890						
	AP	Stan et al., Synchronous Up/Down Counter with Clock Period Independent of Counter Size, Proceedings 13 th IEEE Symposium on Computer Arithmetic, CA, July 6-9, 1997, Pages 274-281, XP00788135						
	AQ	Parhami, Computer Arithmetic Algorithms and Hardware Designs, 2000, Oxford University Press, New York, XP002245799, Sections 5.2 and 5.5, Pages 78-80, 83-85						
EXAMINER:				DATE CONSIDERED:				

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.